AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listing of claims in the application:

LISTING OF CLAIMS:

Claim 1 (Currently amended) An integrated circuit receiver available for infrared or ultrasonic transmission with digital filtering comprising:

an infrared receiver or ultrasonic transducer for receiving a transmitted signal from outside of said integrated circuit receiver and producing a modulated carrier signal at an output thereof;

an amplifier having an input connected to said output of said infrared receiver or ultrasonic transducer for amplifying said modulated carrier signal to ~~be~~ provide an amplified signal at an output of said amplifier; and

a digital filter having an input connected to said output of said amplifier for filtering out a carrier component from said amplified signal to recover an original digital data signal

, said digital filter having a sampling frequency with a period greater than a period of a frequency of said carrier component.

Claim 2 (Currently amended) An integrated circuit receiver according to claim 1, wherein said digital filter ~~comprising~~ includes:

a fixed-interval reset circuit having an input connected to said output of said amplifier for receiving said amplified signal ~~for producing~~ and providing a fetched signal responsive thereto, said fixed-interval reset circuit having a reset period greater than said period of said frequency of said carrier component; and

a fixed-interval sample circuit having an input connected to an output of said fixed-interval reset circuit for ~~demodulating~~ receiving said fetched signal and outputting said original digital data signal responsive thereto, said fixed-interval sample circuit having a sampling period equal to said reset period of said fixed-interval reset circuit.

Claim 3 (Currently amended) An integrated circuit receiver according to claim 2, wherein said fixed-interval reset circuit and fixed-interval sample circuit are constructed with D type flip-flops.

Claim 4 (Currently amended) An integrated circuit receiver according to claim 2, wherein said fixed-interval reset circuit and fixed-interval sample circuit are triggered on a rising edge and falling edge of a clock, respectively.